IN THE CLAIMS

The pending claims are reproduced herein for the Examiner's convenience.

1. (Previously Presented) A computing system comprising:

a processor in a processor package;

a shunt, transient voltage regulator (STVR) in the processor package and coupled to the processor; and

dynamic random-access data storage coupled to at least one of the STVR and the processor.

2. (Original) The computing system of claim 1, further including:

a decoupling capacitor coupled between the processor and the STVR.

3. (Original) The computing system of claim 1, further including:

at least one decoupling capacitor coupled between the processor and the STVR, wherein the at least one decoupling capacitor is selected from a land-side capacitor, a die-side capacitor, and a combination thereof.

4. (Original) The computing system of claim 1, further including:

an interposer coupled to the processor package; and

a decoupling capacitor in the interposer.

5. (Original) The computing system of claim 1, further including:

an interposer coupled to the processor package;

a first decoupling capacitor having a first capacitance functionality in the interposer; and

coupled between the processor and the STVR, a second decoupling capacitor having a second capacitance functionality that is different from the first capacitance functionality.

6. (Original) The computing system of claim 1, further including:

an interposer that is integral with the processor package;

a first decoupling capacitor having a first capacitance functionality in the interposer; and

coupled between the processor and the STVR, a second decoupling capacitor having a second capacitance functionality different from the first capacitance functionality.

7. (Original) The computing system of claim 1, further including:

a mounting substrate, wherein the processor package is coupled to the mounting substrate; and

a DC power converter voltage regulator coupled to the processor in series with the STVR.

8. (Original) The computing system of claim 1, further including:

a mounting substrate, wherein the processor package is coupled to the mounting substrate;

a power socket between the processor and the mounting substrate; and

a DC power converter voltage regulator on the mounting substrate and coupled to the processor in series with the STVR.

9. (Original) The computing system of claim 1, further including:

a mounting substrate, wherein the processor package is coupled to the mounting substrate; and

a DC power converter voltage regulator coupled to the processor in series with the STVR, wherein the DC power converter voltage regulator is optimized for DC power conversion.

10. (Original) The computing system of claim 1, wherein the STVR is optimized for responding to a processor load transient.

11. (Original) The computing system of claim 1, wherein the computing system is disposed in one of a computer, a wireless communicator, a hand-held device, an automobile, a locomotive, an aircraft, a watercraft, and a spacecraft.

12. (Original) The computing system of claim 1, wherein an STVR is coupled to at least one of data storage, a digital signal processor, an application-specific integrated circuit, and a microcontroller.

13. (Previously Presented) An apparatus comprising:

a processor package including:

a processor; and

a shunt, transient voltage regulator (STVR);

a mounting substrate, wherein the processor is coupled to the mounting substrate;

a DC power converter coupled in series with the STVR, to the processor; and

dynamic random-access data storage coupled to at least one of the STVR and the processor.

14. (Original) The apparatus of claim 13, further including:

coupled between the processor and the STVR, a decoupling capacitor.

15. (Original) The apparatus of claim 13, further including:

an interposer coupled to the processor package;

in the interposer, a first decoupling capacitor having a first capacitance functionality; and

coupled between the processor and the STVR, a second decoupling capacitor having a second capacitance functionality that is different from the first capacitance functionality.

16. (Original) The apparatus of claim 13, further including:

between the processor and the mounting substrate, a power socket; and

coupled between the processor and the STVR, a decoupling capacitor in an interposer.

17. (Original) The apparatus of claim 13, wherein the apparatus is disposed in one of a computer, a wireless communicator, a hand-held device, an automobile, a locomotive, an aircraft, a watercraft, and a spacecraft.

18. (Original) The apparatus of claim 13, wherein an STVR is coupled to at least one of data storage, a digital signal processor, an application-specific integrated circuit, and a microcontroller.

19. (Original) A method comprising:

operating a processor in a processor package, wherein the processor package is coupled to at least on of an input/output device; and

with a shunt, transient voltage regulator (STVR) in the processor package, responding to transient loads of the processor.

20. (Original) The method of claim 19, wherein the STVR is operated with an independent voltage source first shunt, and a ground second shunt.

21. (Original) The method of claim 19, further including:

with a DC voltage converter spaced apart from the processor package, converting at least one voltage input to Vcc.

22. (Original) The method of claim 19, further including:

responding to all processor transients with decoupling capacitor functionality selected from a second decoupling capacitor in the processor package, a first decoupling capacitor in an interposer that is coupled to the processor package, a first decoupling capacitor in an interposer that is integral with the processor package, and a combination thereof.

23. (Original) The method of claim 19, wherein the STVR includes an independent voltage source first shunt and a ground second shunt, and further including:

controlling the first shunt and the second shunt by gated logic.

24. (Previously Presented) A method comprising:
inserting a shunt, transient voltage regulator (STVR) in a processor package; and
coupling the processor package to dynamic random-access data storage.

25. (Original) The method of claim 24, further including:
on a mounting substrate for the processor package, coupling in series a DC voltage converter to the STVR.

26. (Original) The method of claim 24, wherein the STVR includes an independent voltage source first shunt, and a ground second shunt.

27. (Original) The method of claim 24, further including:
fabricating a decoupling capacitor in the processor package.

28. (Original) The method of claim 24, further including:
fabricating a decoupling capacitor in an interposer that is integral with the processor package.

29. (Original) The method of claim 24, further including:
between the DC voltage converter and the STVR, inserting a power socket.

30. (Original) The method of claim 24, wherein the STVR is disposed in one of a computer, a wireless communicator, a hand-held device, an automobile, a locomotive, an aircraft, a watercraft, and a spacecraft.

31. (Original)The method of claim 24, wherein an STVR is coupled to at least one of data storage, a digital signal processor, an application-specific integrated circuit, and a microcontroller.